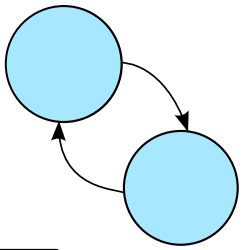
How To Programm FPGA-EBS

Click Here

1. Generate Desing in HDL Designer

- Finite State Machines
- Block Diagrams
- VHDL



.bd
.fm
.vhd
Multiple Source Files

VHDL Source

2. Prepare for Synthesis

Prepare for synthesis

- Generate VHDL Files
- Concatenate VHDL Files
- Trim Libraries

Generate
Concatenate HDL
Trim libs

.vhd chronometer.vhd

3. Launch Xilinx Project Navigator (ISE)

Xilinx Project Navigator

- Synthesize
- Implement Design
- Generate Programming File

Synthesize - XST
Implement Design
Generate Programming File

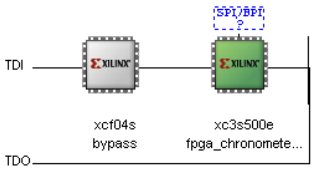
Synthesize → .edif (Netlist) → Place & Route → Generate Programming File

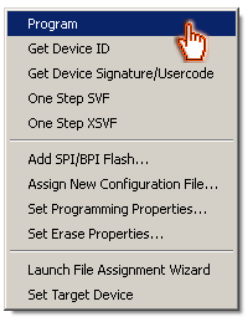
.bit chronometer.bit

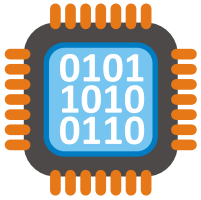
4. Launch Impact

Manage Configuration Project (iMPACT)

- Initialise Chain
- Assign Configuration File
- Program







Congratulations!

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