HEVs
Route du Rawyl 47
1950 Sion 2
www.hevs.ch

Designer:
Zahno Silvan
silvan.zahno@hevs.ch
or
zahno.silvan@gmail.com

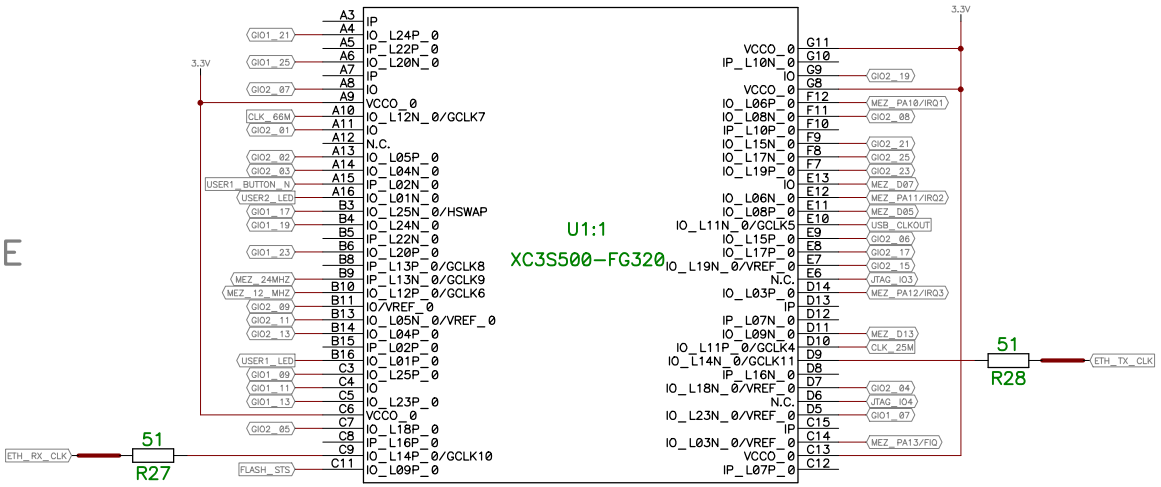
FPGA_EBS Board : Educative FPGA platform

Page	Title	Description
1	Cover	This first page
2	FPGA 1	Xilinx SPARTAN-III FPGA Bank 0 & 1 / Configuration Mode
3	FPGA 2	Xilinx SPARTAN-III FPGA Bank 2 & 3 / Configuration Mode
4	FPGA Alim	Xilinx SPARTAN-III FPGA Alimentation / Decoupling Capacitances
5	FPGA Config	Xilinx EEPROM / JTAG Connectors / FPGA Done LED / Reset Circuit / Source of FPGA programmation
6	Memory	FLASH / SDRAM / Decoupling Capacitances
7	Mezzanine	Mezza A and Mezza B Connectors (mezzanine support)
8	Point-to-point IOs	Crystal Oscillators / User LED / User Button / Test Point / General Purpose connectors
9	Ethernet / RS232	RS232 Circuit / Ethernet interface and Power Over Ethernet
10	Power 1	Power Jack Connector / Voltage Detection / DC DC 5V
11	Power 2	3.3V, 2.5V and 1.2V regulation
12	USB	USB / FPGA dialog over USB / FPGA JTAG over USB

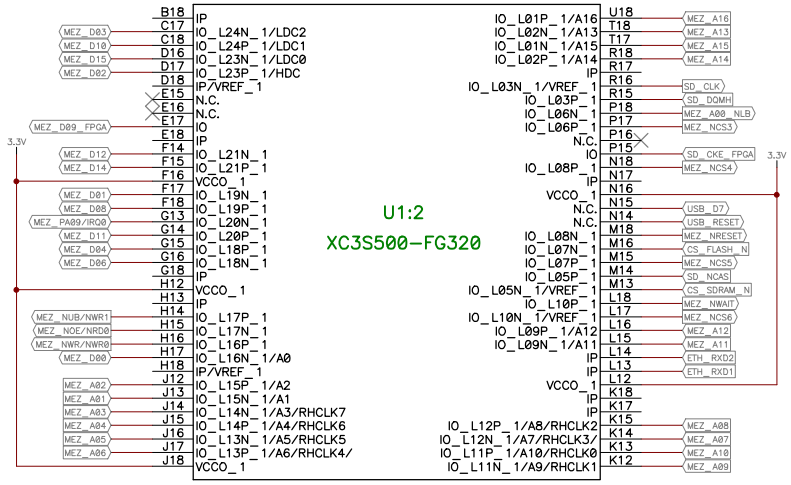
FPGA_EBS Part : Cover	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	1/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

FPGA
SPARTAN – III series
FG320

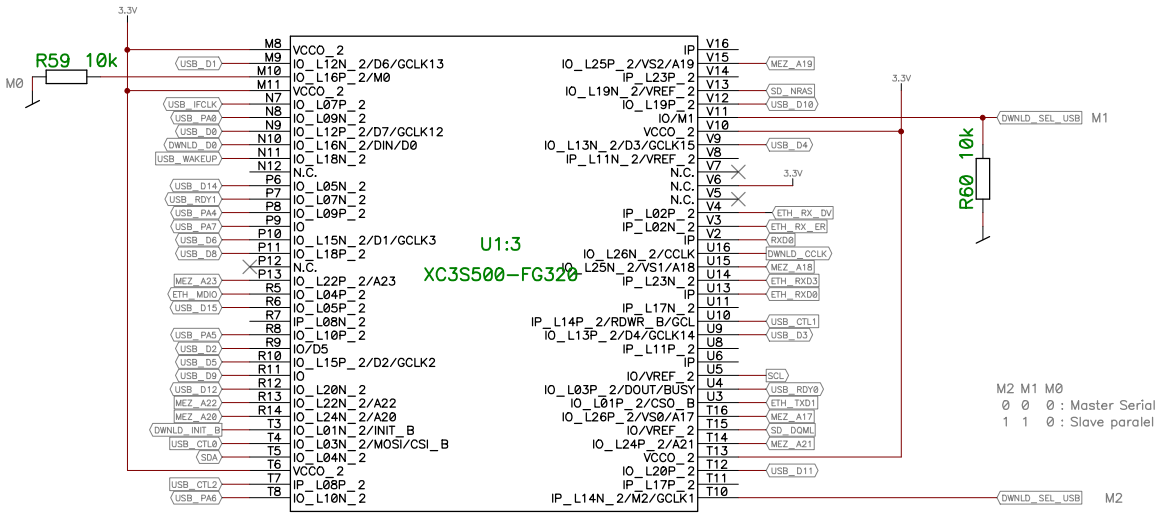
BANK0
TOP SIDE

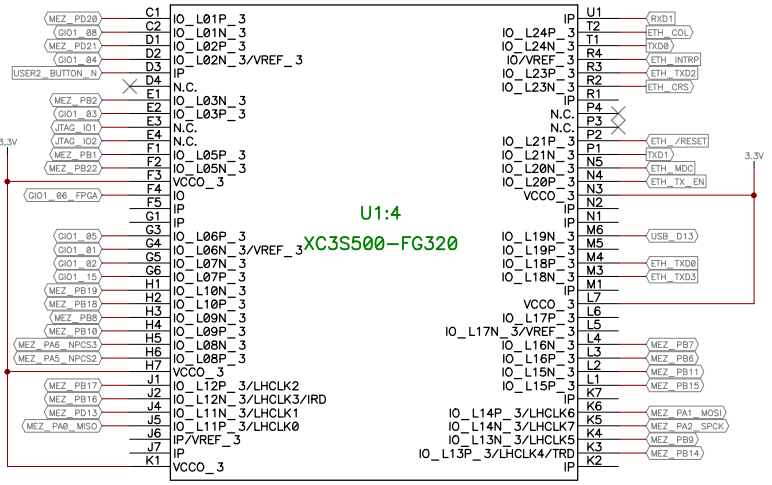


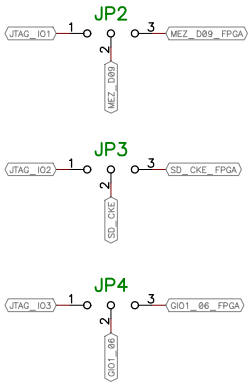
BANK1
RIGHT SIDE



FPGA_EBS		DES	30.06.2014 Zahno Silvan
Part :	FPGA 1	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		2/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

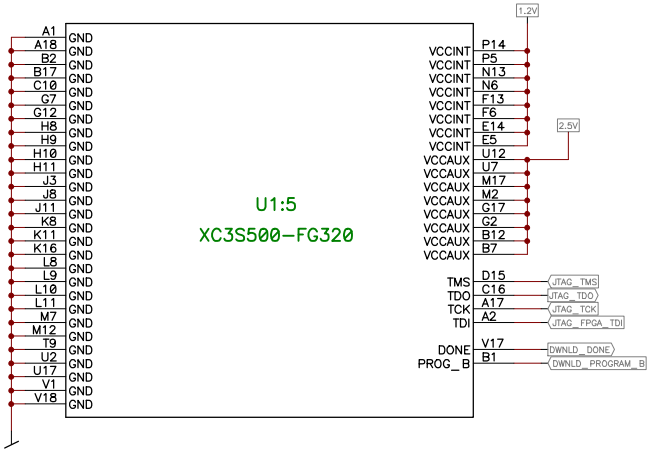


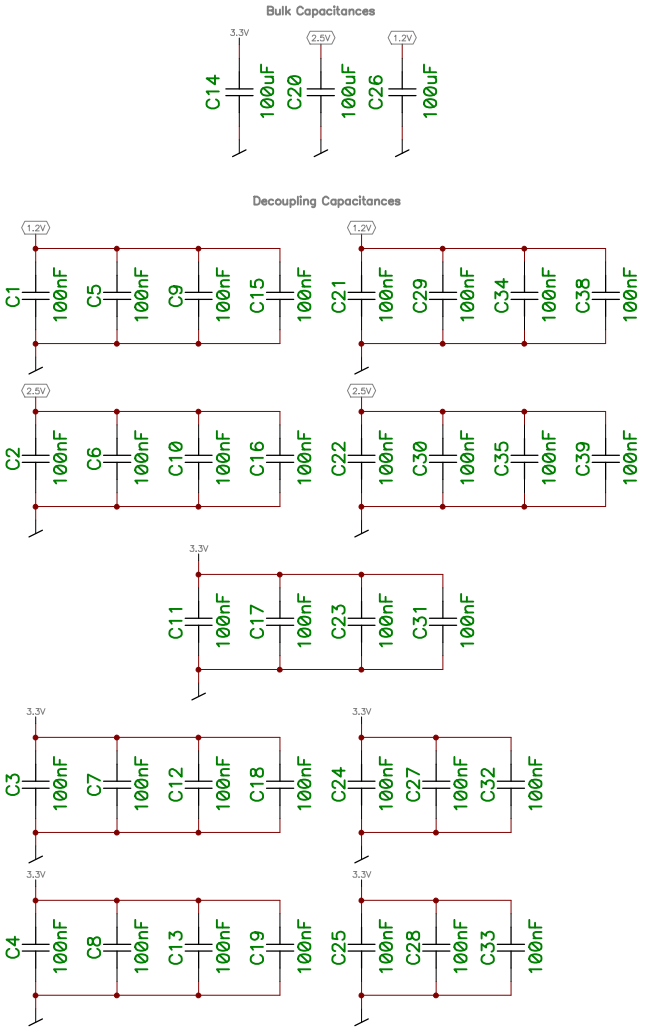




FPGA_EBS Part : FPGA 2	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	3/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

FPGA Capacitances

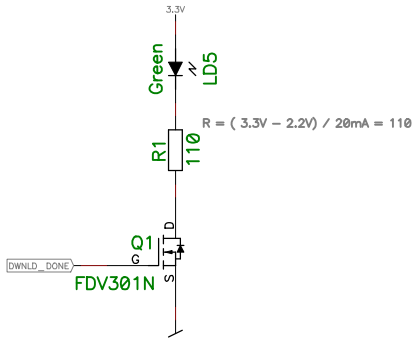




FPGA_EBS	DES	30.06.2014 Zahno Silvan
Part : FPGA Alim	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	4/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

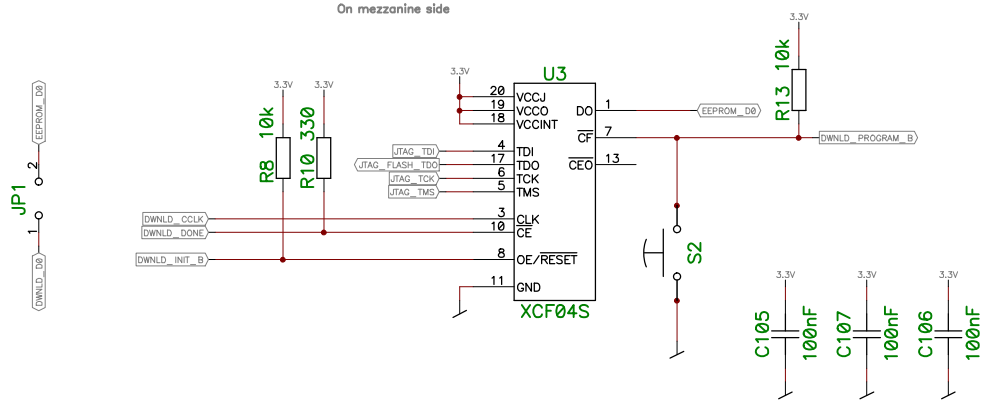
FPGA Done LED

On mezzanine side



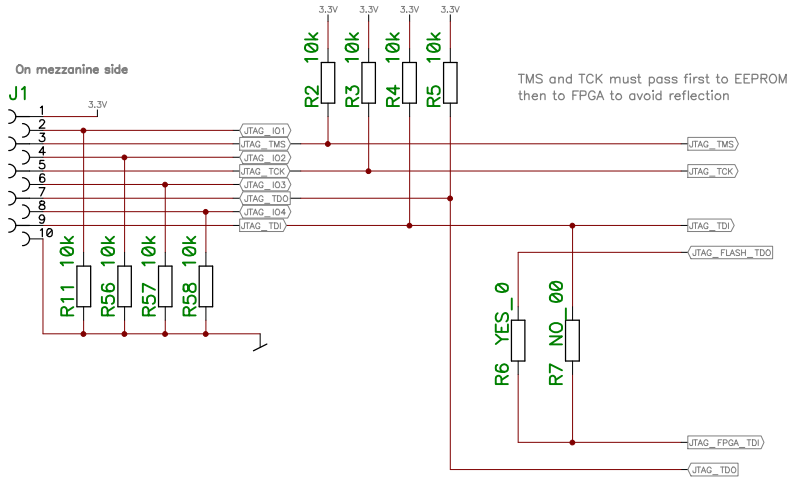
EEPROM for FPGA Configuration

On mezzanine side



JTAG connector

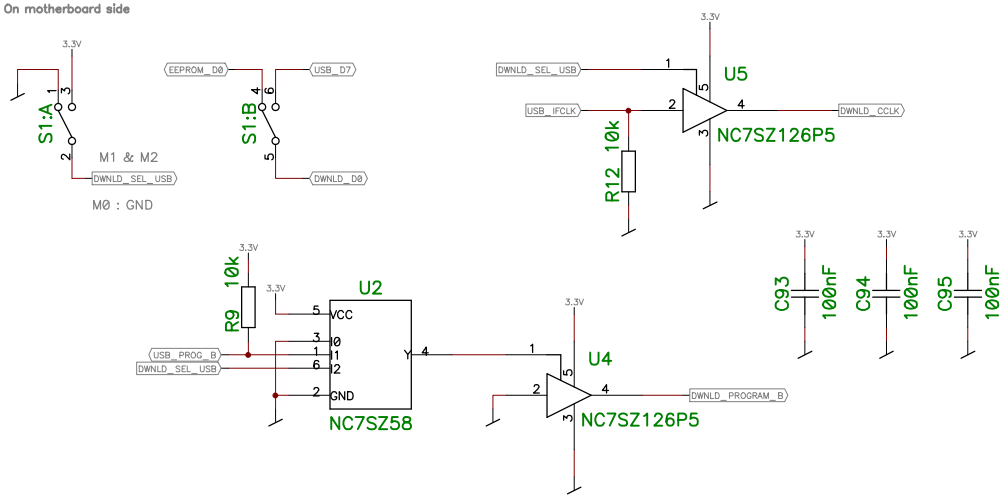
On mezzanine side



Source of programmation of the FPGA

0 0 0 : Master Serial (EEPROM)
1 1 0 : Slave paralell (USB2)
M2 M1 M0

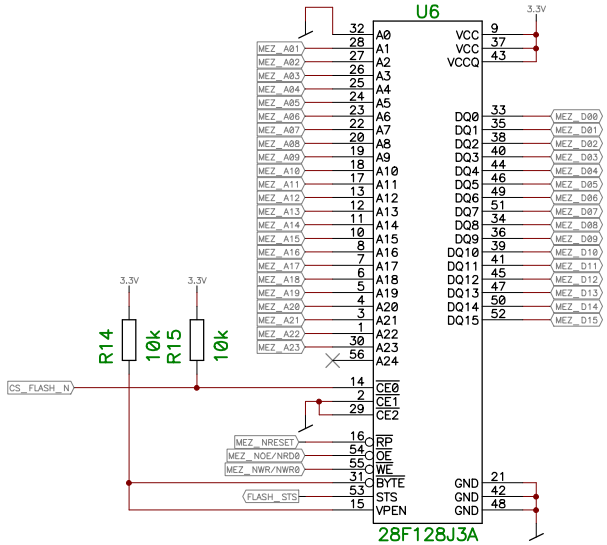
On motherboard side

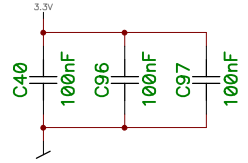


FPGA_EBS Part : FPGA Config	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	5/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

FLASH

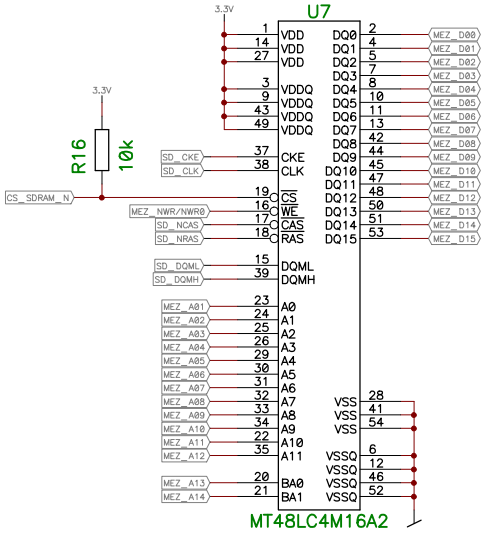
On mezzanine side

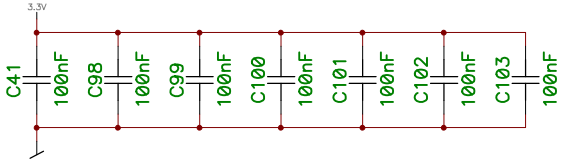




SDRAM

On mezzanine side



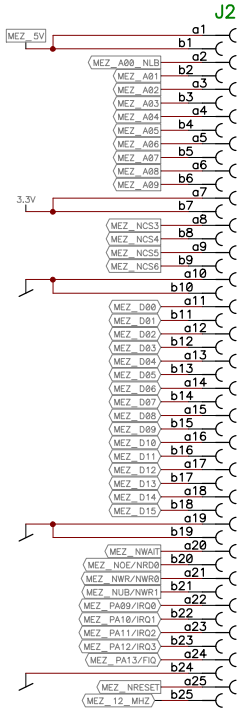


FPGA_EBS Part : Memory	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	6/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

Mezza A

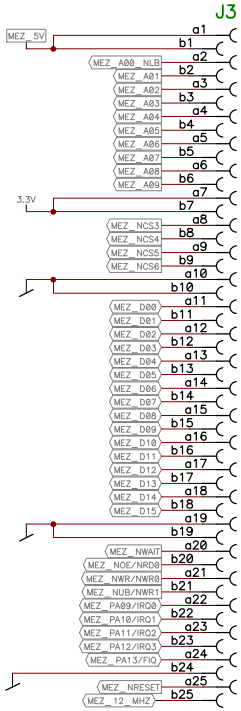
On mezzanine side

TOP SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

BOTTOM SIDE

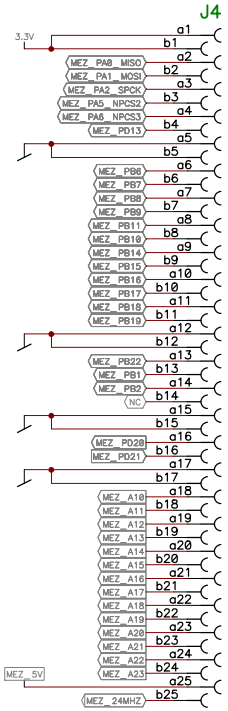


39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

Mezza B

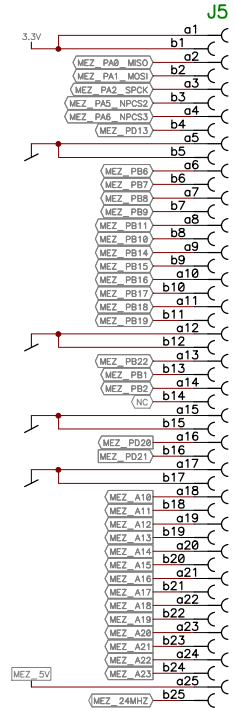
On mezzanine side

TOP SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

BOTTOM SIDE



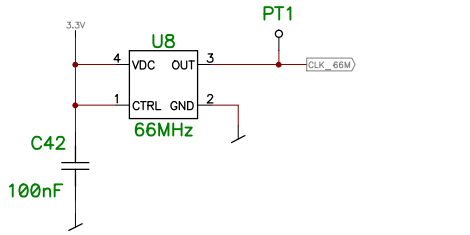
37 point-to-point IOs
+ 1 global clock (MCK0)

FPGA_EBS Part : Mezzanine	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	7/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

Crystal Oscillator

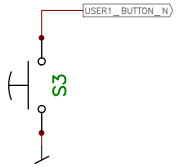
On mezzanine side

Frequency Output Test Point 66MHz



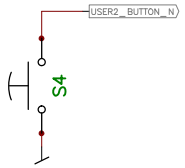
USER1 Button

On mezzanine side



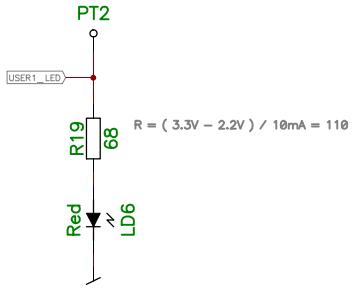
USER2 Button

On mezzanine side



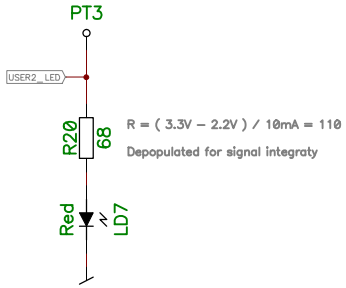
USER1 LED

On mezzanine side



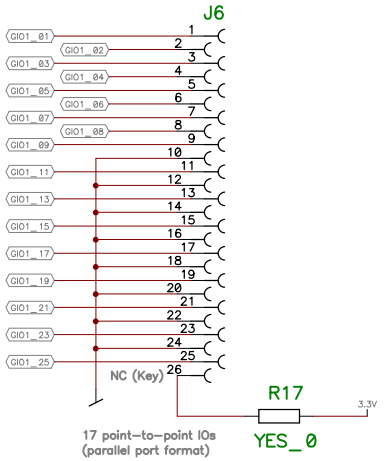
USER2 LED

On mezzanine side



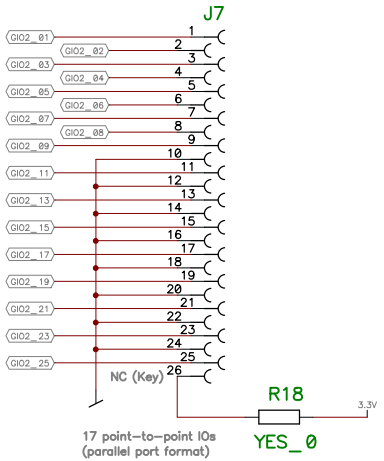
General purpose Connector

On mezzanine side

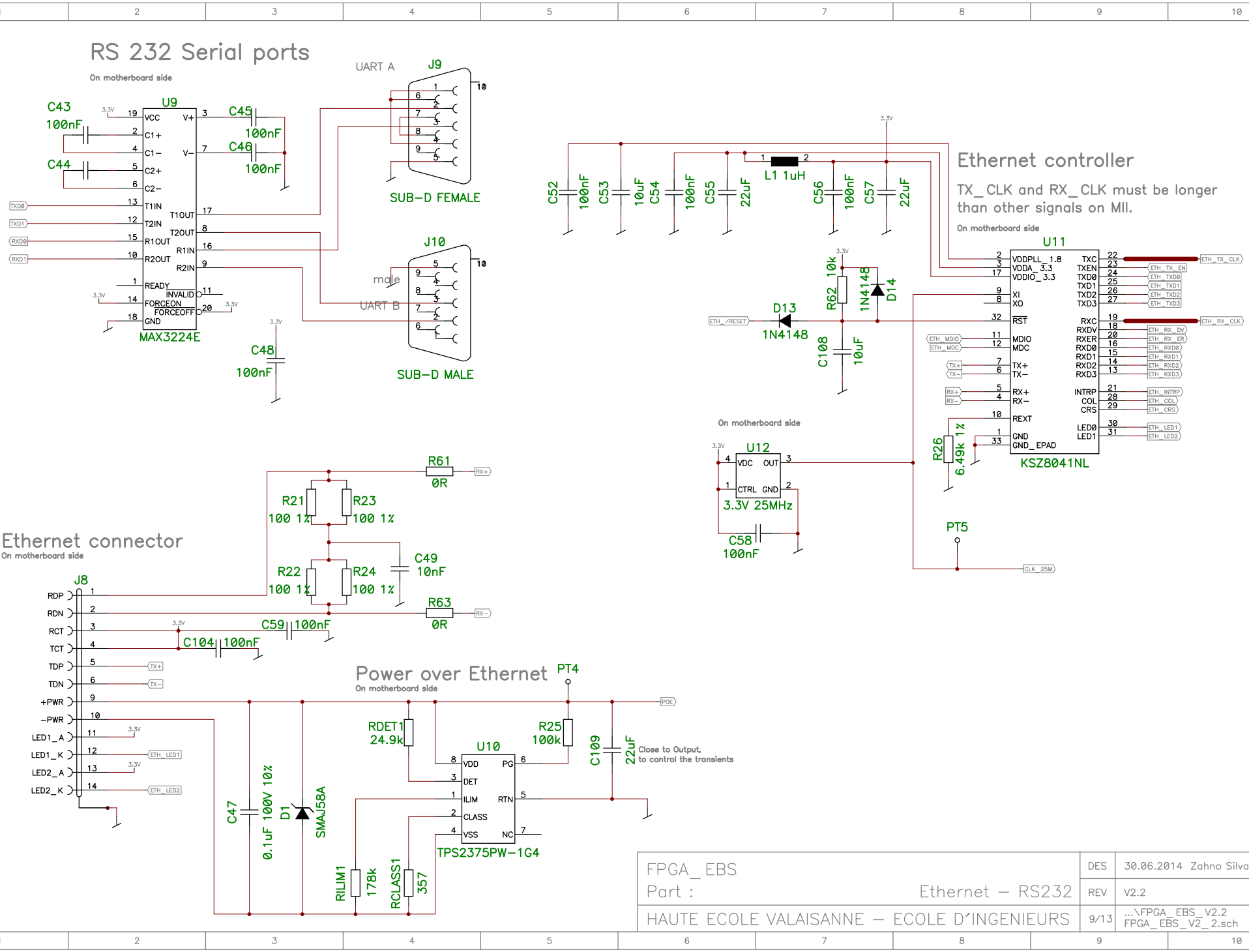


General purpose Connector

On mezzanine side

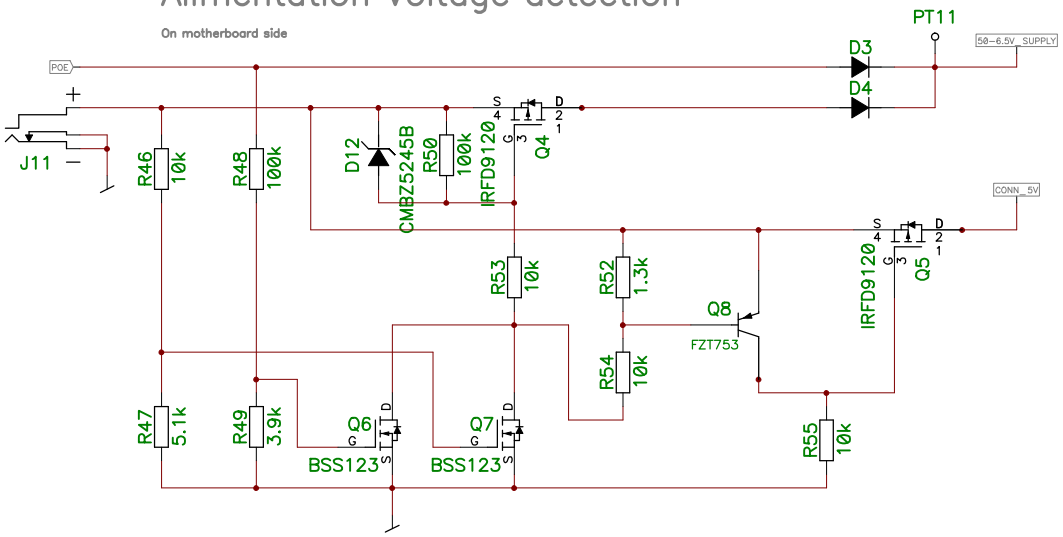


FPGA_EBS Part : Point-to-point IOs	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	8/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch


RS 232 Serial ports
On motherboard side
U9
MAX3224E
C43 100nF
C44
C45 100nF
C46 100nF
C48 100nF
UART A
J9
SUB-D FEMALE
UART B
J10
male
SUB-D MALE
Ethernet controller
TX_CLK and RX_CLK must be longer than other signals on MII.
On motherboard side
U11
KSZ8041NL
L1 1uH
C52 100nF
C53 10uF
C54 100nF
C55 22uF
C56 100nF
C57 22uF
R62 10k
D14 1N4148
D13 1N4148
C108 10uF
R26 6.49k 1%
U12
3.3V 25MHz
C58 100nF
PT5
Ethernet connector
On motherboard side
J8
R61 0R
R21 100 1%
R23 100 1%
R22 100 1%
R24 100 1%
C49 10nF
R63 0R
C59 100nF
C104 100nF
Power over Ethernet
On motherboard side
PT4
U10
TPS2375PW-1G4
RDET1 24.9k
R25 100k
C109 22uF
Close to Output, to control the transients
C47 0.1uF 100V 10%
D1 SMAJ58A
RILIM1 178k
RCLASS1 357
FPGA_EBS
Part :
Ethernet – RS232
DES 30.06.2014 Zahno Silvan
REV V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS
9/13
...\FPGA_EBS_V2.2
FPGA_EBS_V2_2.sch

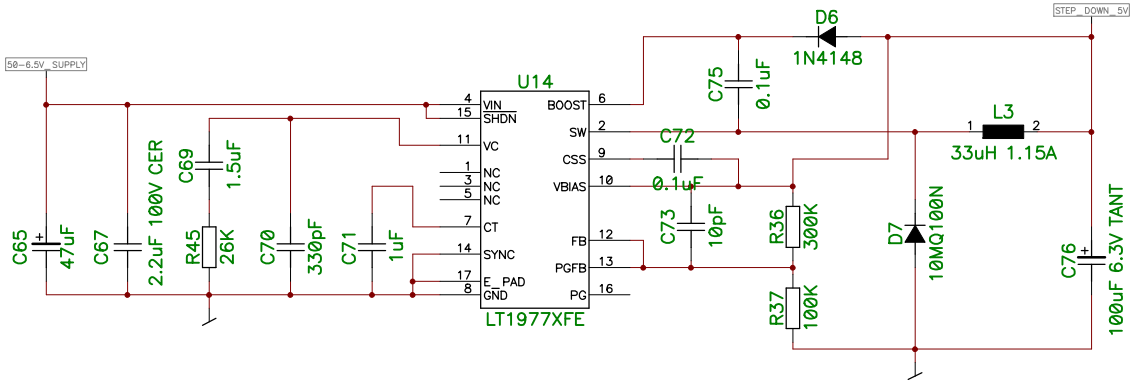
Alimentation Voltage detection

On motherboard side



Power supply 5V/1A from xV

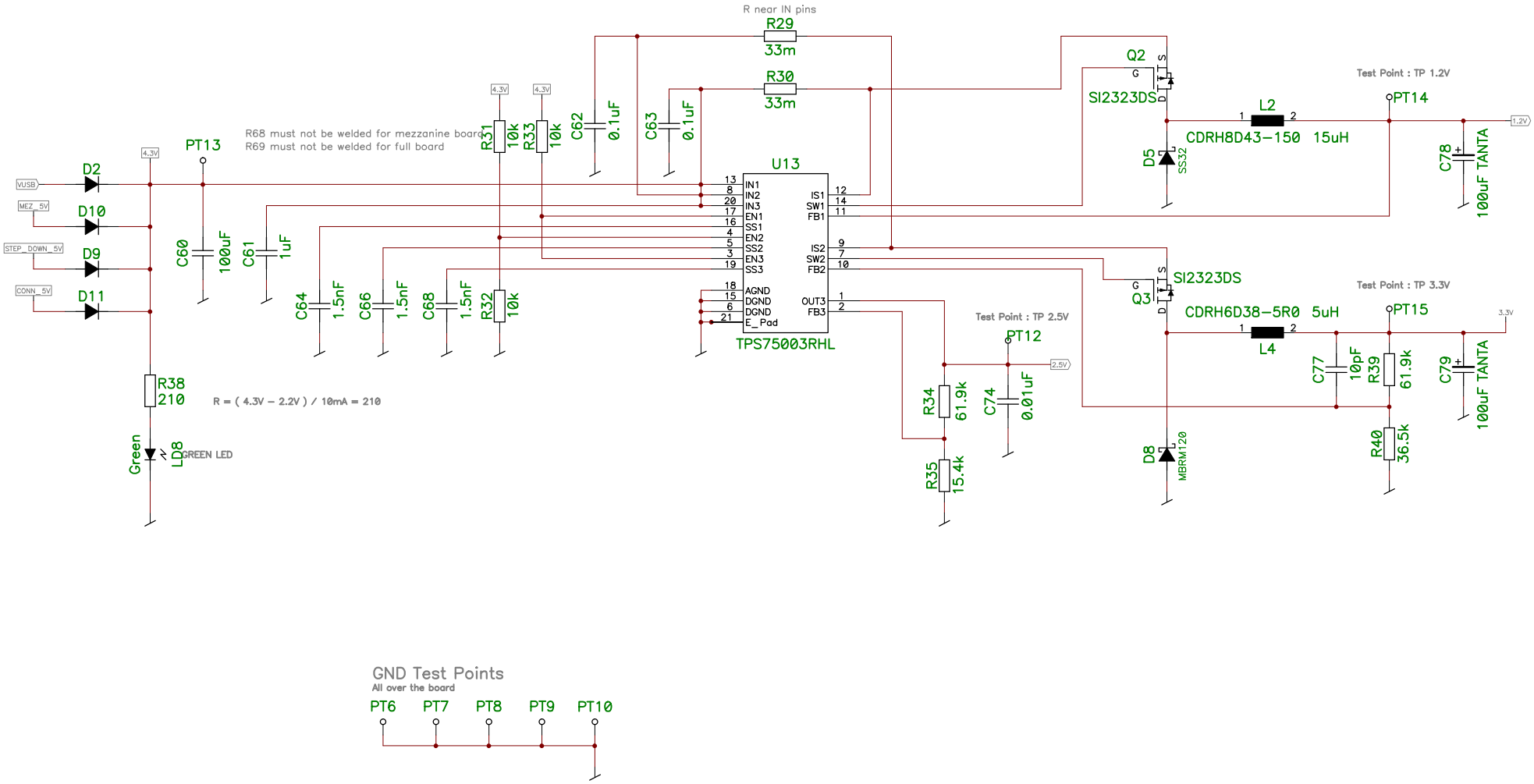
On motherboard side



FPGA_EBS		DES	30.06.2014 Zahno Silvan
Part :	Power 1	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		10/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

Power supply 3.3V, 2.5V and 1.2V from 4.3V

On mezzanine side



GND Test Points

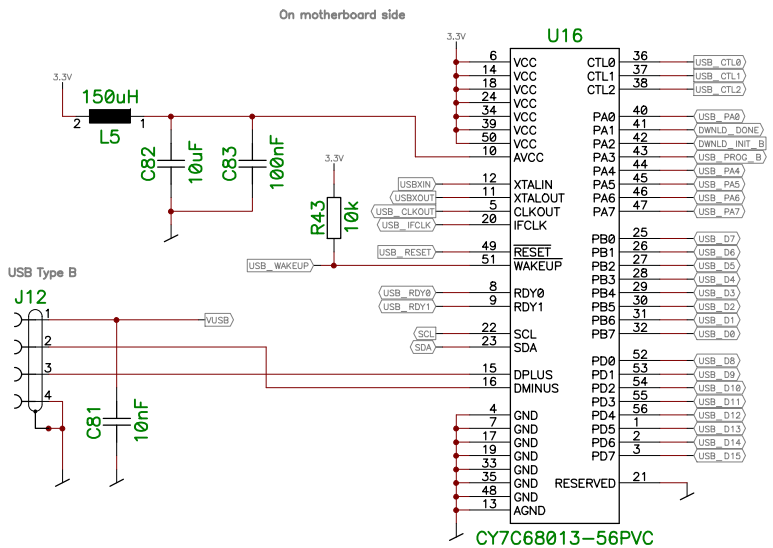
All over the board

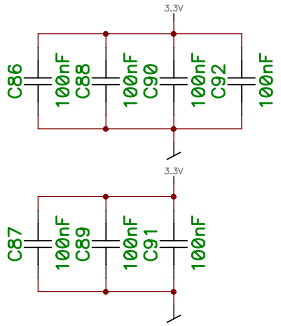
PT6 PT7 PT8 PT9 PT10

FPGA_EBS Part : Power 2	DES	30.06.2014 Zahno Silvan
	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	11/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

USB Controller
Cypress FX2, 8051 processor

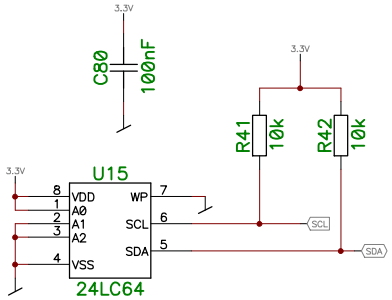
On motherboard side





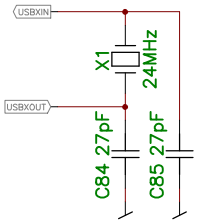
EEPROM for USB 256 x 8

On motherboard side



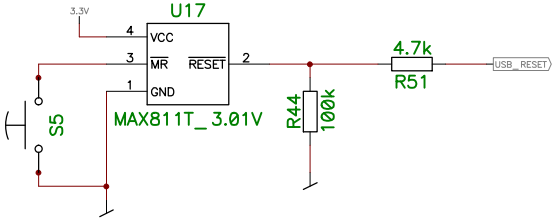
QUARTZ for USB

On motherboard side



Reset for USB

On motherboard side



FPGA_EBS		DES	30.06.2014 Zahno Silvan
Part :	USB	REV	V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		12/13	...\FPGA_EBS_V2.2 FPGA_EBS_V2_2.sch

FPGA_EBS Part : Sheet 13	DES 30.06.2014 Zahno Silvan REV V2.2
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	13/13 ...\FPGA_EBS_V2.2\FPGA_EBS_V2_2.sch